REMARKS

As a preliminary matter, the Examiner is requested to contact the undersigned attorney to schedule an interview after consideration of the above-amendments.

Upon entry of the above amendments, claims 109-112 and 115-131 will be pending. A marked-up version showing the proposed amendments is attached hereto as "**VERSION WITH MARKINGS TO SHOW CHANGES MADE.**"

Claims 110, 116, 117 and 129 were rejected under 35 USC § 112, second paragraph, as being indefinite. It is respectfully submitted that the proposed amendments overcome the informalities noted by the Examiner with respect to these claims.

Claims 18, 19, 36, 41, 43, 87-91 and 97-102 were rejected under 35 USC § 102(e) as being anticipated by ***Kata***. This rejection is rendered moot by the proposed amendment canceling these claims.

Claim 42 was rejected under 35 USC § 102(b) as being anticipated by ***Kata***. This rejection is also rendered moot by the proposed amendment.

Claims 109, 111-114, 117, 118, 121-123 and 131 were rejected under 35 USC § 102(e) as being anticipated by ***Yasunaga***. In addition, claims 115, 119 and 120 were rejected under 35 USC § 103(a) as being unpatentable over ***Yasunaga*** further in combination with ***Nolan***. Favorable reconsideration of these rejections is earnestly solicited.

With respect to claims 109-112, applicants propose amendment to set forth that the external connection protruding electrodes form a bump. The solder 115 shown in Fig. 101A of ***Yasunaga*** merely represents a layer which is plated on the surface of the protruded electrode. Thus, the subject

matter of claims 109-111 is structurally distinct from ***Yasunaga***. By providing such a bump, there is caused a relaxation of stress by both the bump and the part of the protruding electrodes protruding beyond the resin layer. Thereby, the stress relaxation effect is enhanced.

Furthermore, with respect to claims 111 and 112, the end portion of the protruding electrodes is formed to have a convex shape. According to the features set forth in these claims, the adhesion between the bump and the protruding electrode is improved and the stress relaxation effect is enhanced.

When the external connection protruding electrode is a mere layer such as the solder layer 115 of ***Yasunaga***, no stress relaxation effect is expected. Even if a solder layer is provided at the side of the mounting substrate in ***Yasunaga***, the amount of the solder for such a layer is limited and no effective stress relaxation achieved as in the case of using a bump.

The above amendments include a proposal to rewrite claims 115 and 119 in independent form. With respect to these claims applicants respectfully traverse the rejection of the Examiner.

In Figs. 9 and 42 of ***Yasunaga***, the mold sealing process is disclosed wherein it is noted that such a sealing process becomes possible only when the electrode 9 (Fig. 9) or electrode 27 (Fig. 42) is formed of a rigid material like a metal. When these electrodes are formed of a polyamide core covered with a metal film as disclosed in ***Nolan***, the electrode would experience a deformation at the time of the molding process due to the pressure of the resin, and a resin film would be formed on the surface of the electrode in the construction of Fig. 9 or the sealed resin would cause a leak from the cap between the electrode and the mold in the construction of Fig. 42. Thus, a person skilled in the art would never have been motivated to combine the process of ***Yasunaga***, which is applicable only when the electrode is formed of a metal, with the resin core of ***Nolan***.

With regard to claims 121-123, the Examiner states that the peripheral part of the element 113 is thicker than the central part. However, applicants cannot understand this statement of the Examiner. It is noted that Figs. 100, 101A and 101B of ***Yasunaga*** show the element 113 as a semiconductor device, while there is no disclosure at all about the thickness of the chip. Only what is shown in ***Yasunaga*** is a part near the terminal.

Thus, it is believed that the subject matter of claim 121 is not disclosed or suggested in ***Yasunaga***. On the other hand, the proposed amendments to claims 122 and 123 clarify the feature of a part of a side portion of the semiconductor elements being exposed. With this amendment, it is believed that claims 122 and 123 are distinct over ***Yasunaga***.

Claims 124-130 were rejected under 35 USC § 102(b) as being anticipated by ***Nishino***. This rejection is respectfully traversed.

It is noted that claim 124 recites the feature of providing a protrusion used for positioning. ***Nishino***, on the other hand, merely teaches ordinary protruding electrodes and is entirely silent about the protrusion for positioning. By providing such a protrusion for the purpose of positioning separately from the protruding electrodes, it becomes possible to provide the protrusion for positioning at the most suitable locations for positioning, without being constrained by the need of providing electric interconnection.

Thus, the feature of claim 124 is effective and useful for improving the precision of positioning and for improving the easiness of the positioning operation. At the time of dicing operation, for example, the easiness of the positioning operation is facilitated substantially by providing the positioning protrusions in the vicinity of the part where the dicing is actually made. Thereby, the precision of the dicing operation is improved substantially.

With regard to claims 127-131, the Examiner states that ***Nishino*** has the structural feature of "compression-molded."

Applicants respectfully disagree. ***Nishino*** forms the resin on the wafer surface by a spin coating process or a squeeze printing process. As no pressure is applied to the resin at the time of molding, the process of ***Nishino*** is not a compression-molding process.

A compression molding process is defined as a process that includes the step of compressing a sealing resin by reducing the cavity volume. In page 65, lines 18-25 of the present application, there is a description as follows. "The first lower mold half body 23 of the lower mold 22 is maintained in the fixed state. Hence, the volume of the cavity 28 is decreased as the upper mold 12 and the second lower mold half body 24 move in the direction 21. Hence, the sealing resin 35 is compressed and molded in the cavity 28 (the above resin molding method is called compression molding method)".

Hereinafter, the implication of the compression-molding process will be examined in comparison with a transfer molding process as used for achieving a wafer-level packaging of a wafer carrying bumps on the surface thereof.

Generally, a sealing resin contains a large amount of filler particles in an epoxy resin matrix so as to increase the strength of the resin and to lower the thermal expansion coefficient. Because a filler particle has a diameter of several ten microns, the filler particles may be prevented from flowing by the protruding electrodes on the surface of the wafer when a sealing resin is injected according to a transfer molding process, in which process the resin is injected from the lateral side of the wafer.

When this occurs, the resin near the injection gate contains a larger amount of filler particles while the resin far from the gate contains a lesser amount of filler particles. Thus, the composition of the filler particles becomes inhomogeneous and there may occur a difference of strength in the resin layer in a single chip. Further, the thermal expansion coefficient may deviate from the designed value.

In contrast, no such problem occurs when a compressive molding process is employed. In a compression molding process, the sealing resin is compressed while decreasing the volume of the cavity. Thereby, the distance of flow of the resin is minimum and the resin contains a uniform amount of filler particles after the molding process. Thereby, the resin package body has a uniform strength and shows a designed thermal expansion coefficient.

With regard to the implication of the compression-molding process, attached is a copy of ***Kawahara, T., IEEE Trans. Advanced Packaging, vol. 23, no. 2, May 2000, pp. 215-219,*** for facilitating understanding of the Examiner.

In Fig. 8(a) of the reference, it is noted that the features are shown of the post extending from the resin layer and the post having a convex morphology at the tip end thereof.

While ***Nishino*** also teaches a wafer-level packaging process, ***Nishino*** merely uses a spin coating process or squeeze printing process for the formation of the resin layer, contrary to the present invention that uses the compression molding process.

Because of this difference, the present invention can achieve a firm bonding at the interface between the chip surface and the resin layer. Generally, the bonding reaction is facilitated in a resin sealing process when the pressure applied to the resin is increased. In the case of spin-coating process or squeeze printing process, on the other hand, no substantial pressure is applied to the resin

layer at the time of formation thereof. Thus, the package of ***Nishino*** has an inherent weakness with regard to the bonding between the resin layer and the chip.

According to the invention as set forth in the present application, the resin is compressed at the time of the resin layer formation. Thus, the bonding strength at the interface between the resin layer and the chip surface is improved and a package suitable for practical use is obtained.

It is also noted that, in the case of the compression molding process, heating of the resin is conducted simultaneously to the compressing process. Thus, the bonding reaction at the resin layer and the chip surface is much more facilitated as compared with the spin coating process or squeeze printing process, in which the heating process is conducted after a liquid form resin is applied.

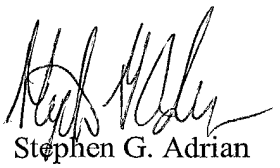
For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by Applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone Applicants' undersigned attorney.

In the event that this paper is not timely filed, applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



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VERSION WITH MARKINGS TO SHOW CHANGES MADE S. N. 09/029,608

IN THE CLAIMS:

Claims 109-111, 115-117, 119, 122, 123 and 129 have been amended.

109. (Amended) A semiconductor device comprising:

a semiconductor element having a surface on which protruding electrodes are formed;

a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof; and

external connection protruding electrodes provided to the end portions of the protruding electrodes that protrude from the resin layer,

said external connection protruding electrodes forming a bump.

110. (Amended) The semiconductor device as claimed in claim [108] 109, wherein the resin layer and the semiconductor element have surfaces defined by cutting using a dicer.

111. (Amended) A semiconductor device comprising:

a semiconductor element having a surface on which protruding electrodes having convex end portions are formed;

a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except the convex end portions thereof; and

external connection protruding electrodes provided to the convex end portions of the protruding electrodes that protrude from the resin layer,

said external connection protruding electrodes forming a bump.

115. (Amended) [The semiconductor device as claimed in claim 113,] A semiconductor device comprising :

a semiconductor element having a surface on which protruding electrodes are formed; and

a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof,

the protruding electrodes having a core portion and an electrically conductive film formed on a surface of the protruding core portion,

wherein the core portion comprises an elastic resin.

116. (Amended) The semiconductor device as claimed in claim [114] 115, wherein the elastic resin is polyimide.

117. (Amended) A semiconductor device comprising:

a semiconductor element having a surface on which protruding electrodes are formed;

a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof; and

external connection protruding electrodes provided to the end portions of the protruding electrodes that protrude from the resin layer,

the protruding electrodes having a core portion and an electrically conductive film formed on a surface of the [protruding] core portion.

119. (Amended) [The semiconductor device as claimed in claim 117,] A semiconductor device comprising:

a semiconductor element having a surface on which protruding electrodes are formed;

a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof; and

external connection protruding electrodes provided to the end portions of the protruding electrodes that protrude from the resin layer,

the protruding electrodes having a core portion and an electrically conductive film formed on a surface of the protruding core portion,

wherein the core portion comprises an elastic resin.

122. (Amended) A semiconductor device comprising :

a semiconductor element having a surface on which protruding electrodes are formed; and

a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof,

the semiconductor element having an outer peripheral portion that is thicker than a central portion thereof,

a part of a side portion of said semiconductor elements being exposed.

123. (Amended) A semiconductor device comprising :

a semiconductor element having a surface on which protruding electrodes are formed; and

a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof,

a part of a side portion of the semiconductor element being covered with the resin layer, a part of a side portion of said semiconductor elements being exposed.

129. (Amended) The semiconductor device as claimed in claim 128, wherein [the] a side surface of the resin layer and [the] a side surface of the semiconductor element are flush with each other.